15W High-Integration, High-Efficiency PMIC for Wireless Power Transmitter

- VIN Input Voltage Range: 4.2V-20V
- PVIN Input Voltage Range: 1V-15V
- Up to 15W Power Transfer
- Integrated Full-Bridge Power Stage with 16-m Rdson of Power MOSFETs
- Integrated 5V-100mA LDO
- Optimized for EMI Reduction
- Integrated 33KHz~133KHz

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V_{IN}=V_{PVIN1}=V_{PVIN2}=12V, typical value is tested under 25°C.

SYMBOL	PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
Input supplies and UVLO						
V_{IN}						

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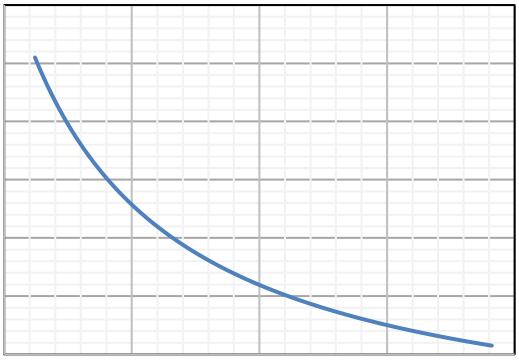

Figure 2. Clock Frequency VS FREQ Resistor

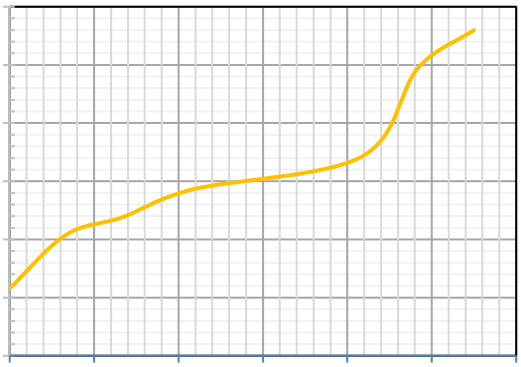

Figure 3. Frequency VS Temperature

Figure 4. VDD VS Temperature

Figure 5. 5V LDO Iout vs Vout

Figure 6. Input Quiescent current VS Temperature

Figure 7. Full bridge Ron VS Temperature

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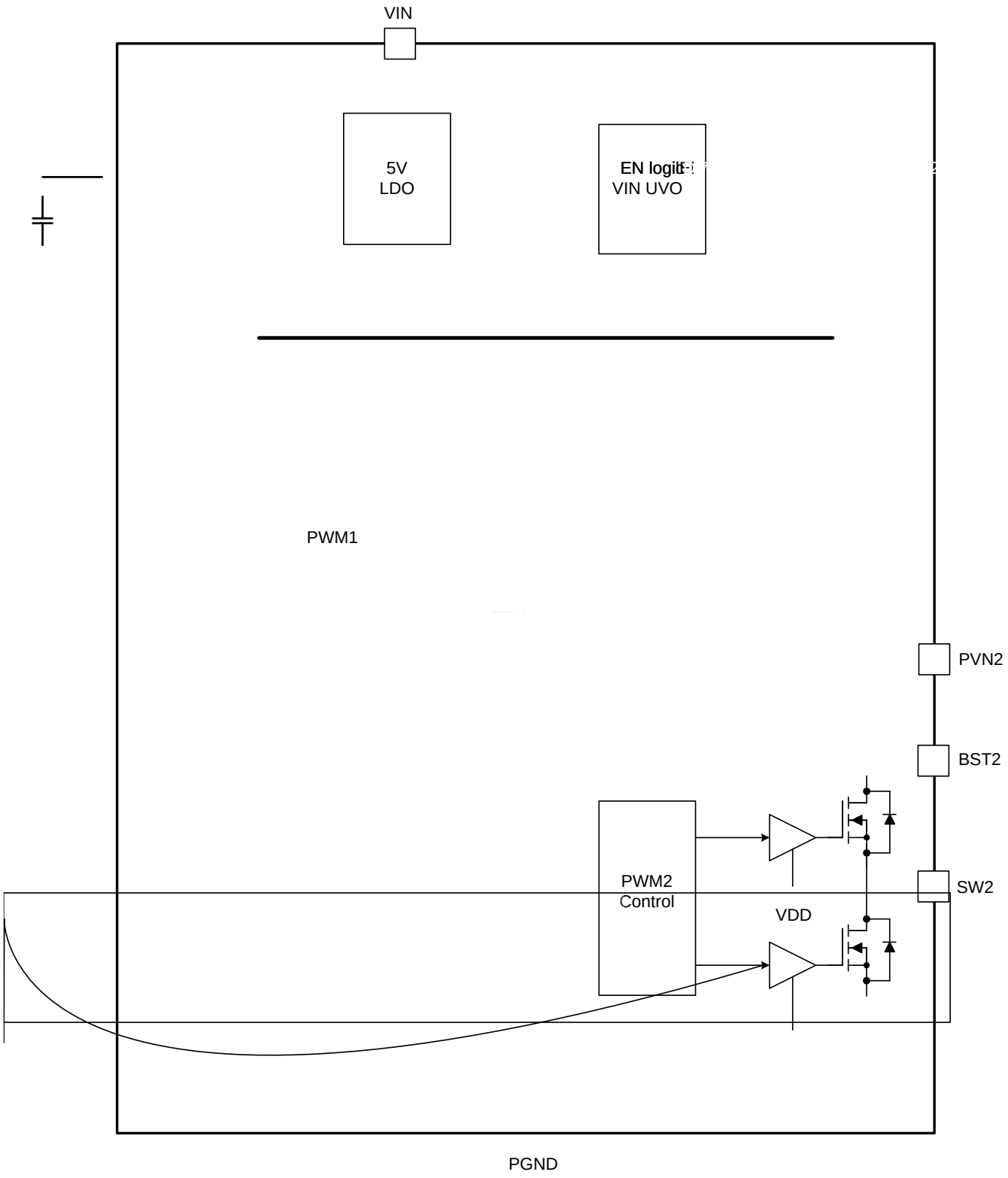

Figure 8. Functional Block Diagram

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5V LDO

The SCT63141 has an integrated low-dropout voltage regulator which powered from VIN and supply regulated 5V voltage on VDD pin. The output current capability is 100mA. This LDO can be used to bias the supply voltage of external transmitter controller directly.

It is recommended to connect a decoupling ceramic capacitor of 1uF to 10uF to the VDD pin. Capacitor values outside of the range may cause instability of the internal linear regulator.

Clock Generator

The SCT63141 has an integrated clock generator to produce two complementary clock signals to control the full bridge power. The duty cycle of the output clock signals is fixed 50% while the frequency of the clock can be configured through an external resistor connecting from FREQ pin to GND pin. The frequency configuration range is from 33KHz to 132KHz. The transmitted power can be configured by adjusting the frequency of clock on the basis of the LC resonant frequency and also the power requirement from receiver. Use Equation 3 or the table1 to determine the resistance for a switching frequency needed.

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PWM1 input controls the half bridge comprised of high side MOSFET Q1 and low side MOSFET Q2, and PWM2 input controls the half bridge comprised of high side MOSFET Q3 and low side MOSFET Q4 as shown in block diagram. The PWM1 and PWM2 independently control the SW1 and SW2. Logic HIGH will turn off low side FET and turn on high side FET, and logic LOW will turn off high side FET and turn on low side FET.

An external 100nF ceramic bootstrap capacitor between BST1 and SW1 pin powers floating high-side power MOSFET Q1's gate driver, and the other 100nF bootstrap capacitor between BST2 and SW2 pin powers for the Q3's. When low side FET is on which means SW is low, the bootstrap capacitor is charged through internal path by VDD power supply rail.

Full Bridge Over Current Protection

The SCT63141 integrates cycle-by-cycle current limit and hiccup mode for over-current protection. The current of the high side FET Q1and Q3 is sensed and compared to the current limit threshold during each switching cycle. If the current exceeds the threshold, 12.5A typical, the high side FET turns off immediately in present cycle to avoid current increasing even PWM signal is still kept in high level. The over current counter is incremented. If one high side FET occurs over current in 5 consecutive cycles, then all 4 internal FETs are turned off regardless of the PWM inputs. The full bridge enters hiccup mode and will attempt to restart after a time-out period of 24ms typically.

Operational Amplifier

The SCT63141 has an operational amplifier with two differential input pins OPIP and OPIN with OPO as the output pin. The power supply of this amplifier is VDD. Amplifier output has 8.5mA max current limit both from VDD to OPO and also from OPO to GND. The amplifier can be used as signal amplification or be configured to a comparator for silicon photodiode signal demodulation.

Thermal Shutdown

The SCT63141 protects the device from the damage during excessive heat and power dissipation condition. Once the junction temperature exceeds 155°C, the thermal sensing circuit stops two LDOs and full bridge of 4-MOSFETs' working. When the junction temperature falls below 120°C, then the device restarts.

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Typical Application

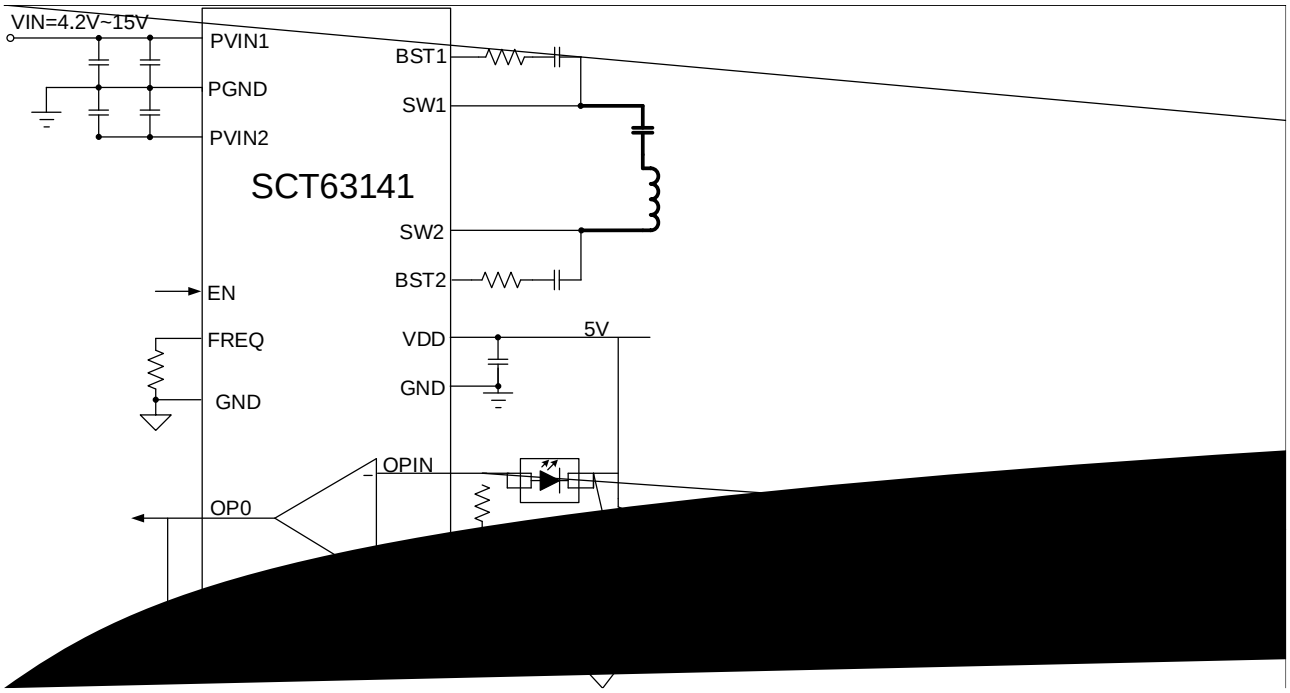

Figure 10. Wireless Power System

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Layout Guideline

Proper PCB layout is a critical for SCT63141 For better results, follow these guidelines as below:

1. Bypass capacitors from PVIN to PGND should put next to PVIN and PGND pin as close as possible especially for the two small capacitors.
2. PGND connect to bottom layer by via between capacitors.
3. Bypass capacitors from VIN to GND should put next to VIN and GND pin as close as possible especially for the small capacitor.
4. Bypass capacitor for VDD place next to VDD pin.

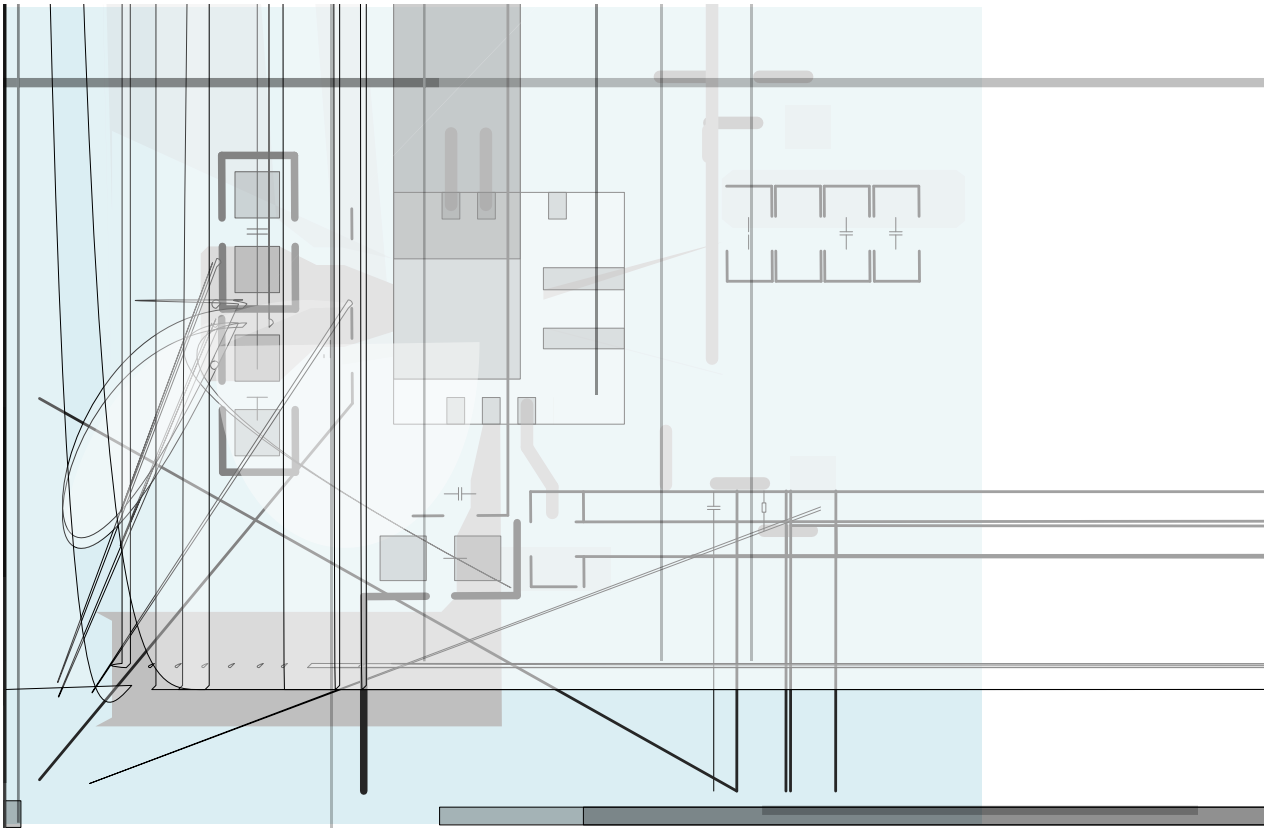

Figure 17. PCB Layout Example

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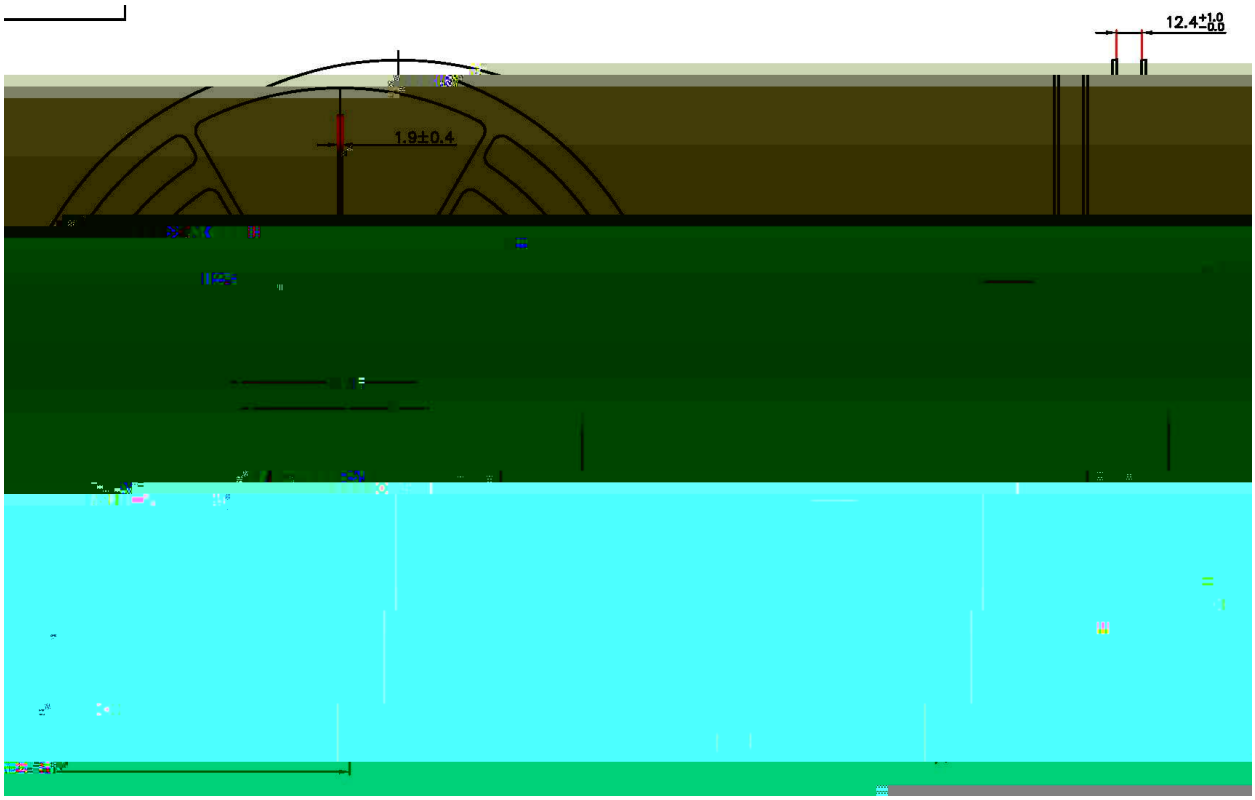

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