# 15W High-Integration, High-Efficiency PMIC for Wireless Power Transmitter

- VIN Input Voltage Range: 4.2V-20V
- PVIN Input Voltage Range: 1V-15V
- Up to 15W Power Transfer
- Integrated Full-Bridge Power Stage with 16-m Rdson of Power MOSFETs
- Integrated 5V-100mA LDO
- Optimized for EMI Reduction
- Build-in 3.3V-100mA LDO
- Integrated Lossless Input Current Sensor with ±2% accuracy for FOD and current Demodulation
- 3.3V and 5V PWM Signal Logic Compatible
- Input Under-Voltage Lockout
- Over Current Protection
-

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| | | |
|---|---|---|
| BST2 | 8 | Power supply bias for the high-side power MOSFET gate driver of Q3 as shown in the block diagram. Connect a 0.1uF capacitor from BST2 pin to SW2 pin. |
| SW2 | 9 | Switching node of the half-bridge FETs Q3 and Q4. |
| SW1 | 10 | Switching node of the half-bridge FETs Q1 and Q2. |
| BST1 | 11 | Power supply bias for the high-side power MOSFET gate driver of Q1 as shown in the block diagram. Connect a 0.1uF capacitor from BST1 pin to SW1 pin. |
| EN | 12 | Enable pin. Pull the pin high or keep it floating to enable the IC. When the device is enabled, 5V LDO will start to work if VIN higher than UVLO threshold. After VDD is established, power stage responds to PWM input logic then. |
| ISNS | 13 | Current detection output. The voltage of the pin is proportional to the input current. |
| PWM2 | 14 | PWM logic input to the FET Q3 and Q4 as shown in the Block Diagram. Logic HIGH turns off the low-side FET Q4, and turns on the high-side FET Q3. Logic LOW turns off the high-side FET Q3 and turns on the low-side FET Q4. When PWM input is in the tri-state mode, both Q3 and Q4 are turned off. |
| PWM1 | 15 | PWM logic input to the FET Q1 and Q2 as shown in the Block Diagram. Logic HIGH turns off the low-side FET Q2, and turns on the high-side FET Q1. Logic LOW turns off the high-side FET Q1 and turns on the low-side FET Q2. When PWM input is in the tri-state mode, both Q1 and Q2 are turned off. |

Over operating free-air temperature range unless otherwise noted

| PARAMETER | DEFINITION | MIN | MAX | UNIT |
|---|---|---|---|---|
| $V_{IN}$ | Input voltage range | 4.2 | 20 | V |
| $P_{VIN}$ | Input voltage range | 1 | 15 | V |
| $T_J$ | Operating junction temperature | -40 | 125 | °C |

| PARAMETER | DEFINITION | MIN | MAX | UNIT |
|---|---|---|---|---|
| $V_{ESD}$ | Human Body Model(HBM), per ANSI-JEDEC-JS-001-2014 specification, all pins(1) | -2 | +2 | kV |
| | Charged Device Model(CDM), per ANSI-JEDEC-JS-002-2014specification, all pins(2) | -1 | +1 | kV |

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

| PARAMETER | THERMAL METRIC | DFN-19L | UNIT |
|---|---|---|---|
| R | Junction to ambient thermal resistance(1) | 48 | °C/W |
| R | Junction to case thermal resistance(1) | 45 | |

(1) SCT provides R and R numbers only as reference to estimate junction temperatures of the devices. R and R are not a characteristic of package itself, but of many other system level characteristics such as the design and layout of the printed circuit board (PCB) on which the SCT63140 is mounted, thermal pad size, and external environmental factors. The PCB board is a heat sink that is soldered to the leads of the SCT63140. Changing the design or configuration of the PCB board changes the efficiency of the heat sink and therefore the actual R and R .

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$V_{PVIN1}$=$V_{PVIN2}$=12V, VDD=5V, typical value is tested under 2

| SYMBOL | PARAMETER | | MIN | | MAX | UN |
|---|---|---|---|---|---|---|
| **Input supplies and UVLO** | | | | | | |
| $V_{IN}$ | Operating input voltage | | 4.2 | | 20 | V |
| $P_{VIN}$ | Operating input voltage | | 1 | | 15 | V |
| $V_{IN_UVLO}$ | $V_{IN}$ UVLO Threshold<br>Hysteresis | | | | | V<br>m |
| $V_{DD_UVLO}$ | $V_{DD}$ UVLO Threshold<br>Hysteresis | | | 440 | | V<br>m |
| $I_{SHDN}$ | Shutdown current from VIN pin | EN=0V, VIN=12V | | 1 | | A |
| | Shutdown current from PVIN1,PVIN2 | EN=0V, PVIN=12V | | 1 | 3 | u |
| $I_{VINQ}$ | Quiescent current from VIN pin | EN floating, VDD=5V, no loading on LDO | | 300 | | u |
| $I_{PVINQ}$ | | EN floating, VDD=5V, no loading on LDO | | 50 | | u |

**ENABLE INPUTS and PWM logic**

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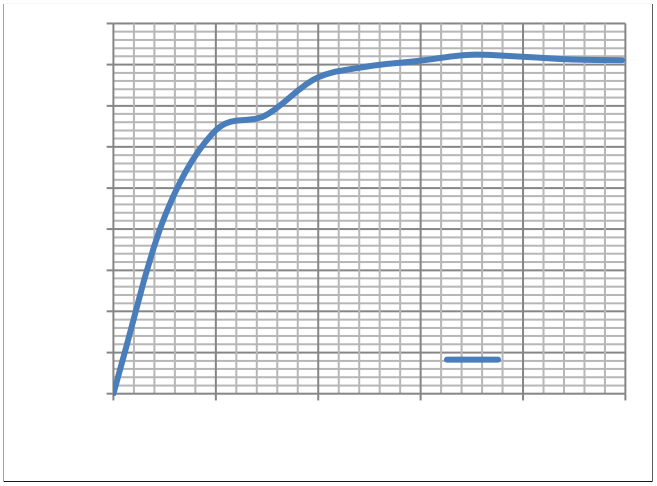

Figure 2. Transfer Efficiency with 5W RX@ Vout=5V

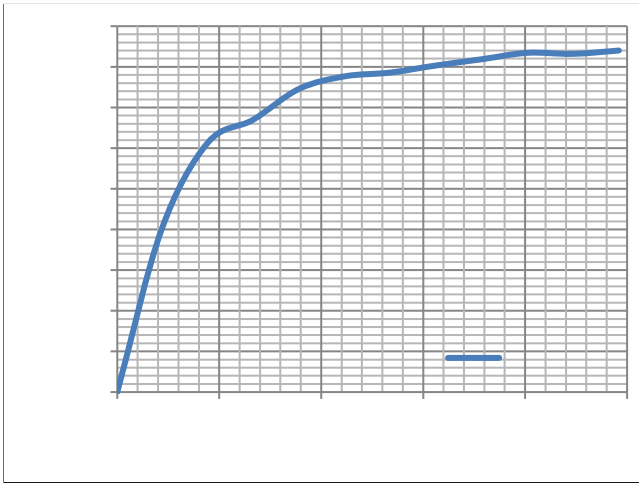

Figure 3. Transfer Efficiency with 10W RX@ Vout=9V

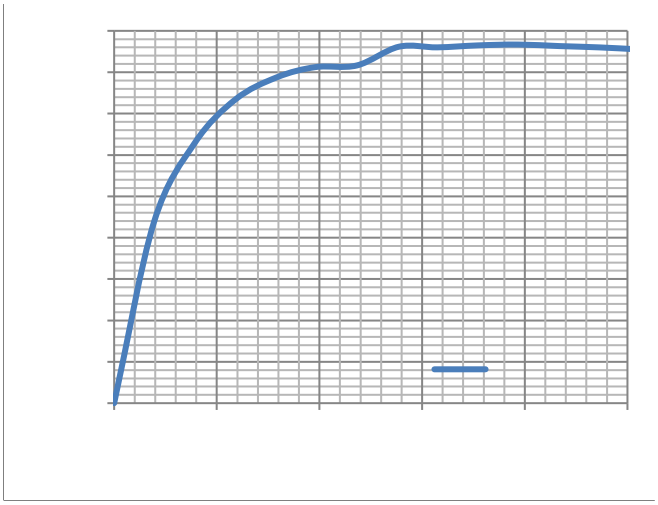

Figure 4. Transfer Efficiency with 15W RX@ Vout=12V

Figure 5. 5V LDO Iout vs Vout

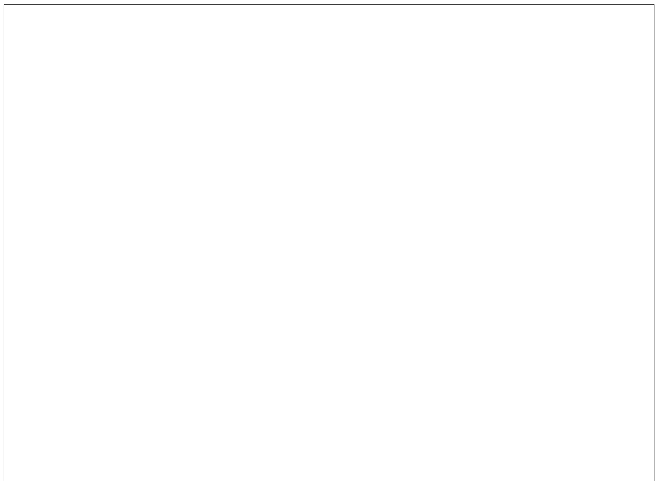

Figure 6. 3.3V LDO Iout vs Vout

Figure 7. Current Sense Output Voltage vs Iin

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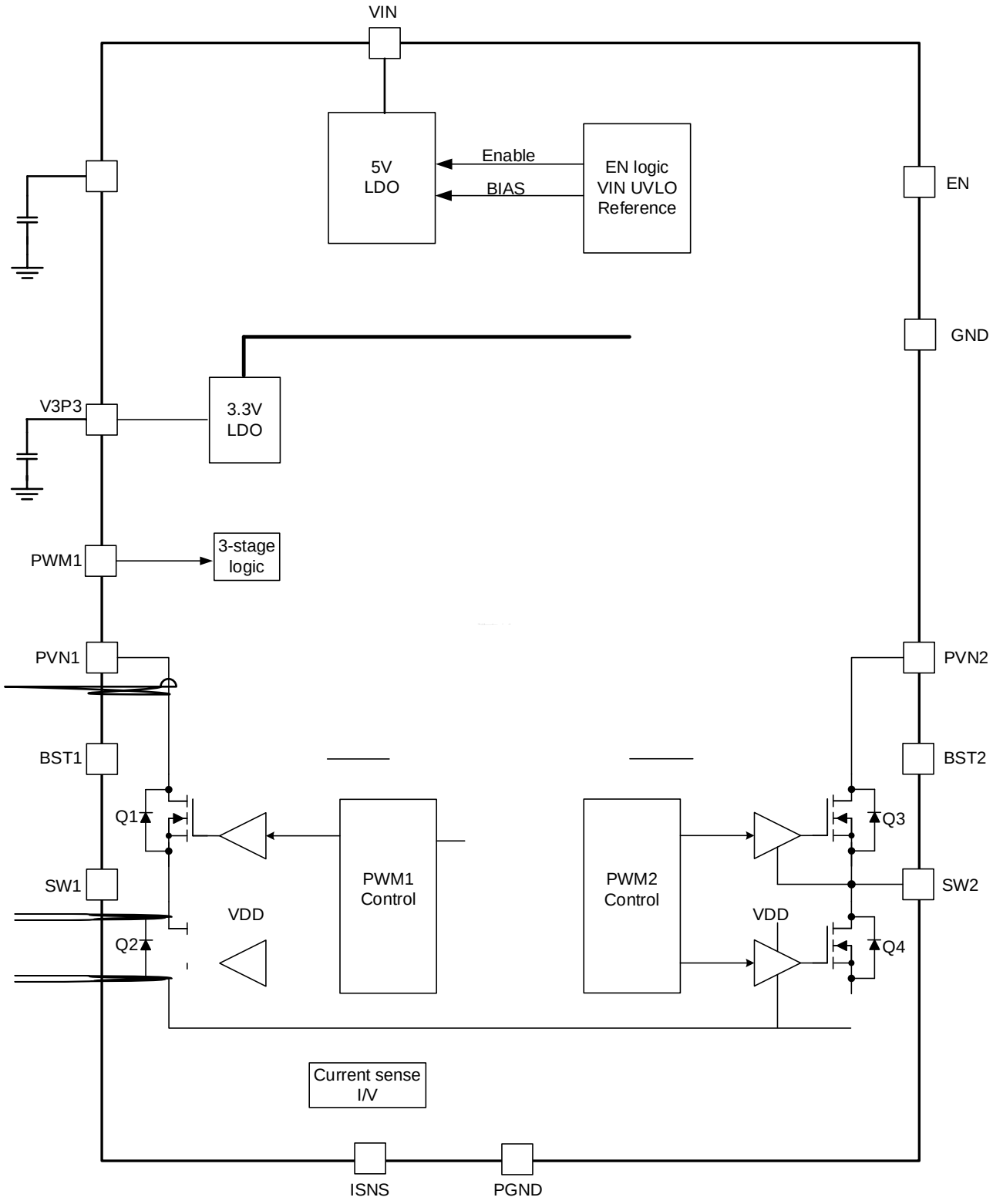


**Figure 8. Functional Block Diagram**

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### 3.3V LDO

The SCT63140 has an integrated low-dropout voltage regulator which powered from VDD and supply regulated 3.3V voltage on V3V pin. The output current capability is 100m EOlu ty is

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## Application Waveforms

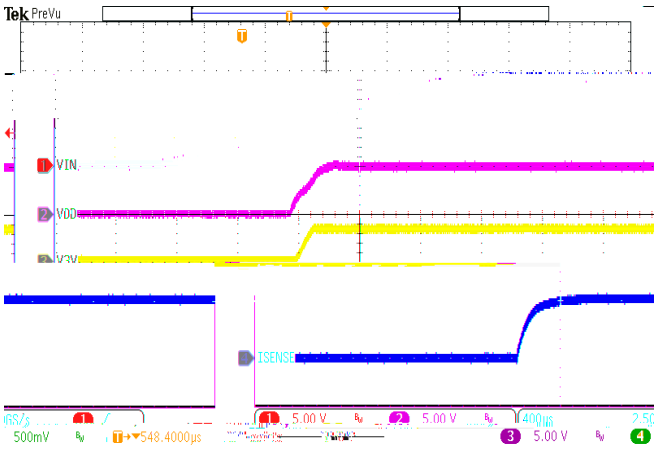


Figure 12. Power Up

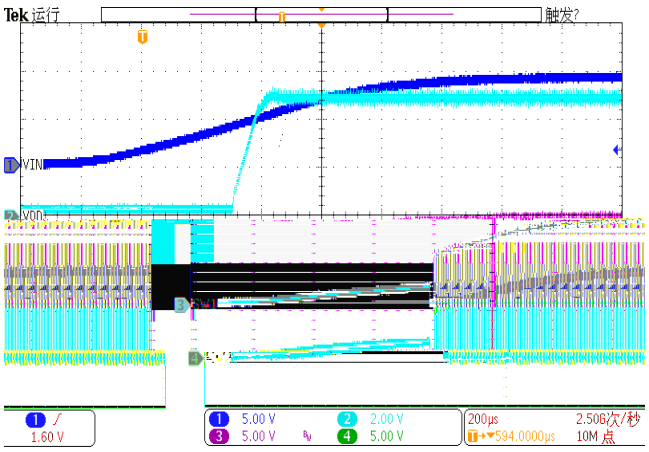


Figure 13. Power Up

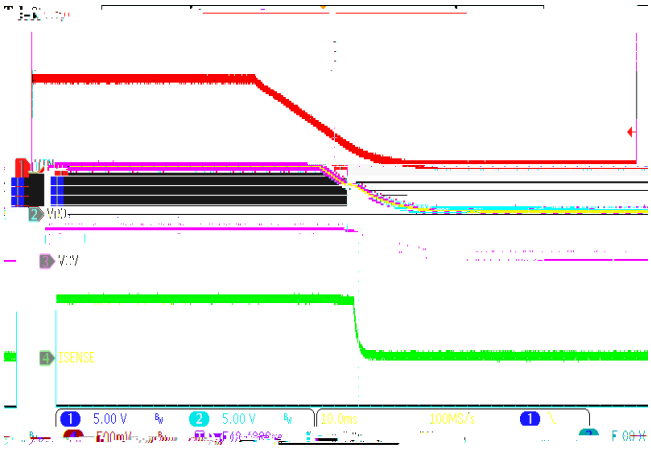


Figure 14. Power Down

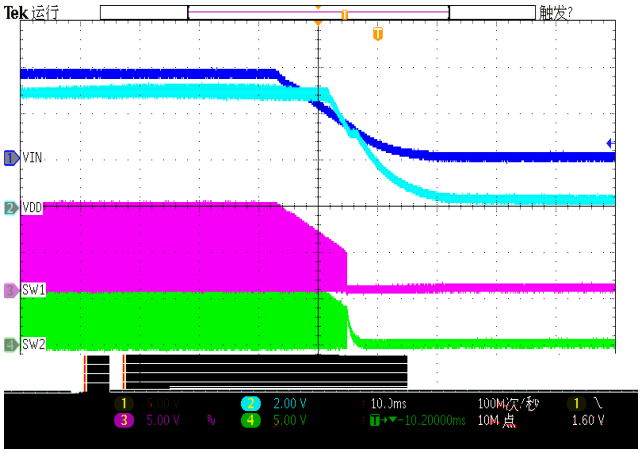


Figure 15. Power Down

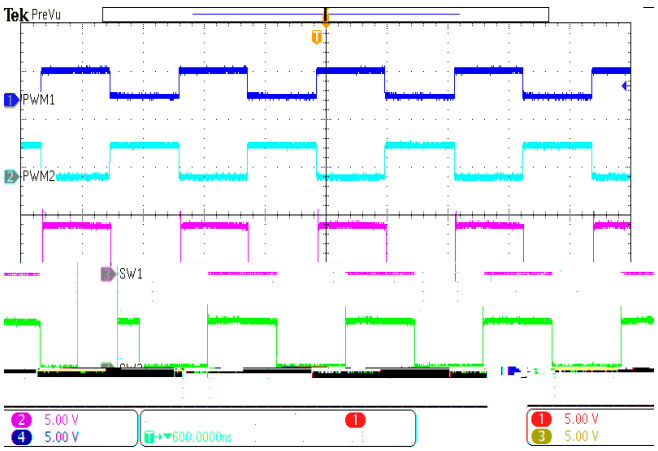


Figure 16. Full bridge @Vin=5V, RX=5W

Figure 17. Full bridge @Vin=9V, RX=10W

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**Layout Guideline**

Proper PCB layout is a critical for SCT63140 For better results, follow these guidelines as below:

1. Bypass capacitors from PVIN to PGND should put next to PVIN and PGND pin as close as possible especially for the two small capacitors.
2. PGND connect to bottom layer by via between capacitors.
3. Bypass capacitors from VIN to GND should put next to VIN and GND pin as close as possible especially for the small capacitor.
4. Bypass capacitor for VDD place next to VDD pin.
5. Bypass capacitor for V3V place next to V3V pin.

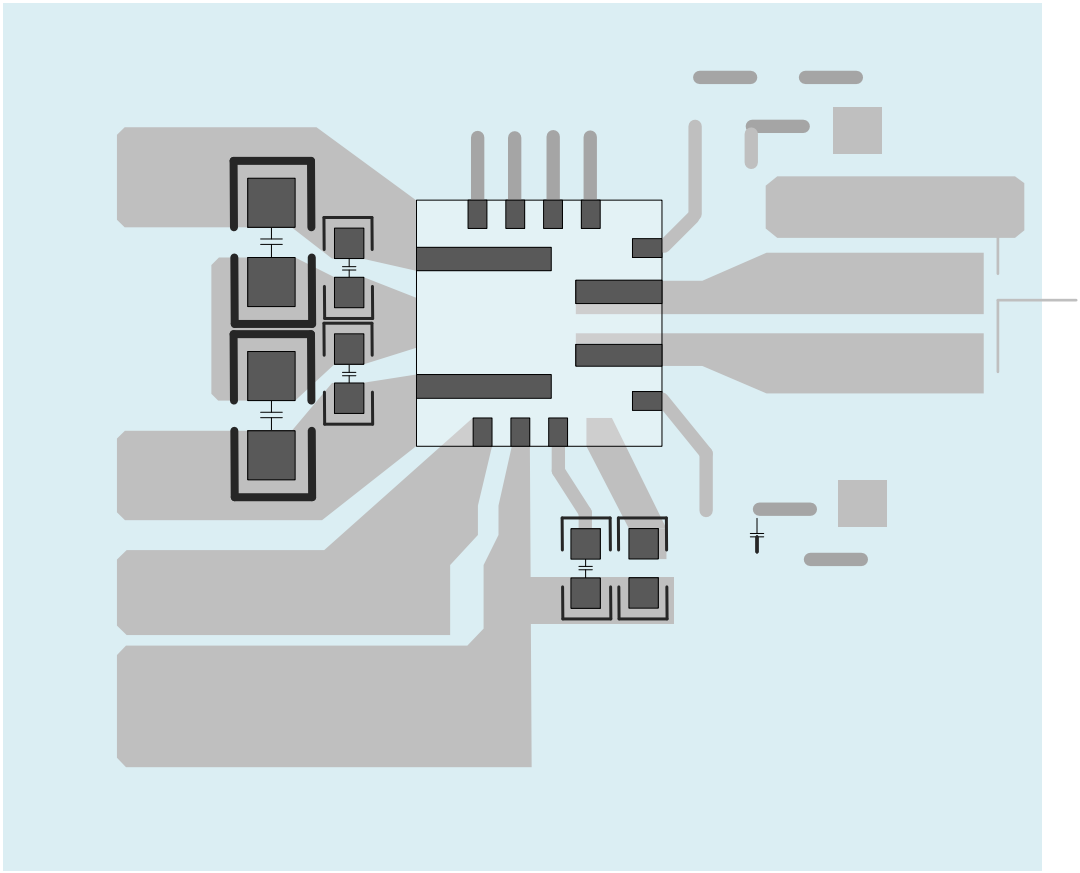

Figure 18. PCB Layout Example

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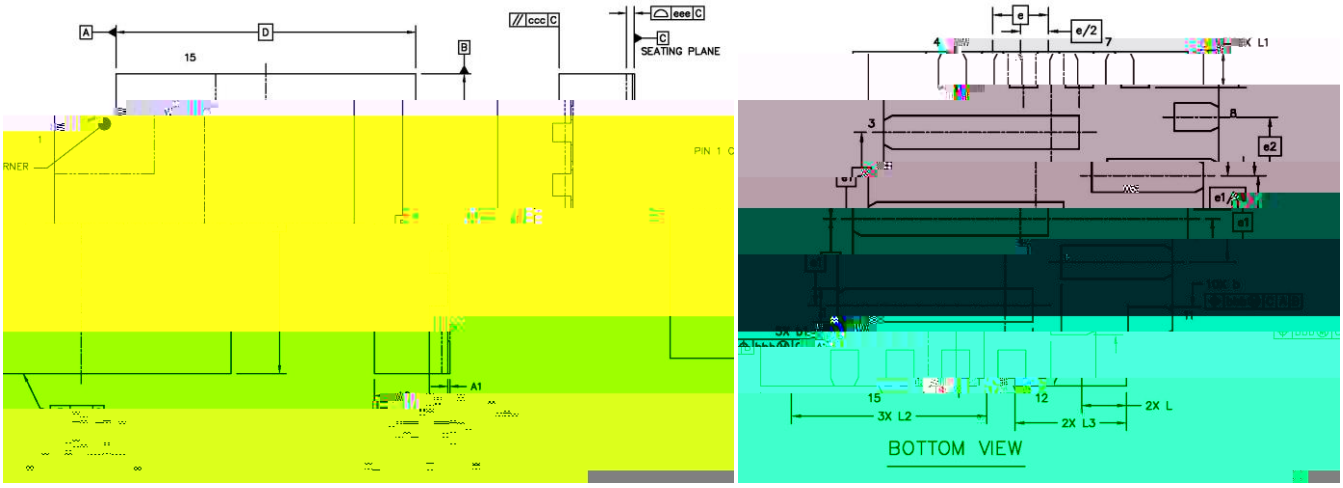


FCQFN-15L (3x3) Package Outline Dimensions

| | | Symbol | Dimensions in Millimeters | | |
|---|---|---|---|---|---|
| | | | Min. | Nom. | Max. |
| TOTAL THICKNESS | | A | 0.70 | 0.75 | 0.80 |
| STAND OFF | | A1 | 0 | 0.02 | 0.05 |
| MOLD THICKNESS | | A2 | | 0.55 | |
| L/F THICKNESS | | A3 | | 0.203 REF | |
| LEAD WIDTH | | b | 0.20 | 0.25 | 0.30 |
| | | b1 | 0.25 | 0.30 | 0.35 |
| BODY SIZE | X | D | | 3.00 BSC | |
| | Y | E | | 3.00 BSC | |
| LEAD PITCH | | e | | 0.50 BSC | |
| | | e1 | | 0.775 BSC | |
| | | e2 | | 0.525 BSC | |
| LEAD LENGTH | | L | 0.30 | 0.40 | 0.50 |
| | | L1 | 0.225 | 0.325 | 0.425 |
| | | L2 | 1.65 | 1.75 | 1.85 |
| | | L3 | 0.90 | 1.00 | 1.10 |
| PACKAGE EDGE TOLERANCE | | aaa | | 0.1 | |
| MOLD FLATNESS | | ccc | | 0.1 | |
| COPLANARITY | | eee | | 0.08 | |
| LEAD OFFSET | | bbb | | 0.1 | |

**NOTE:**

1. Drawing proposed to be made a JEDEC package outline MO-220 variation.
2. Drawing not to scale.
3. All linear dimensions are in millimeters.
4. Thermal pad shall be soldered on the board.
5. Dimensions of exposed pad on bottom of package do not include mold flash.
6. Contact PCB board fabrication for minimum solder mask web tolerances between the pins.

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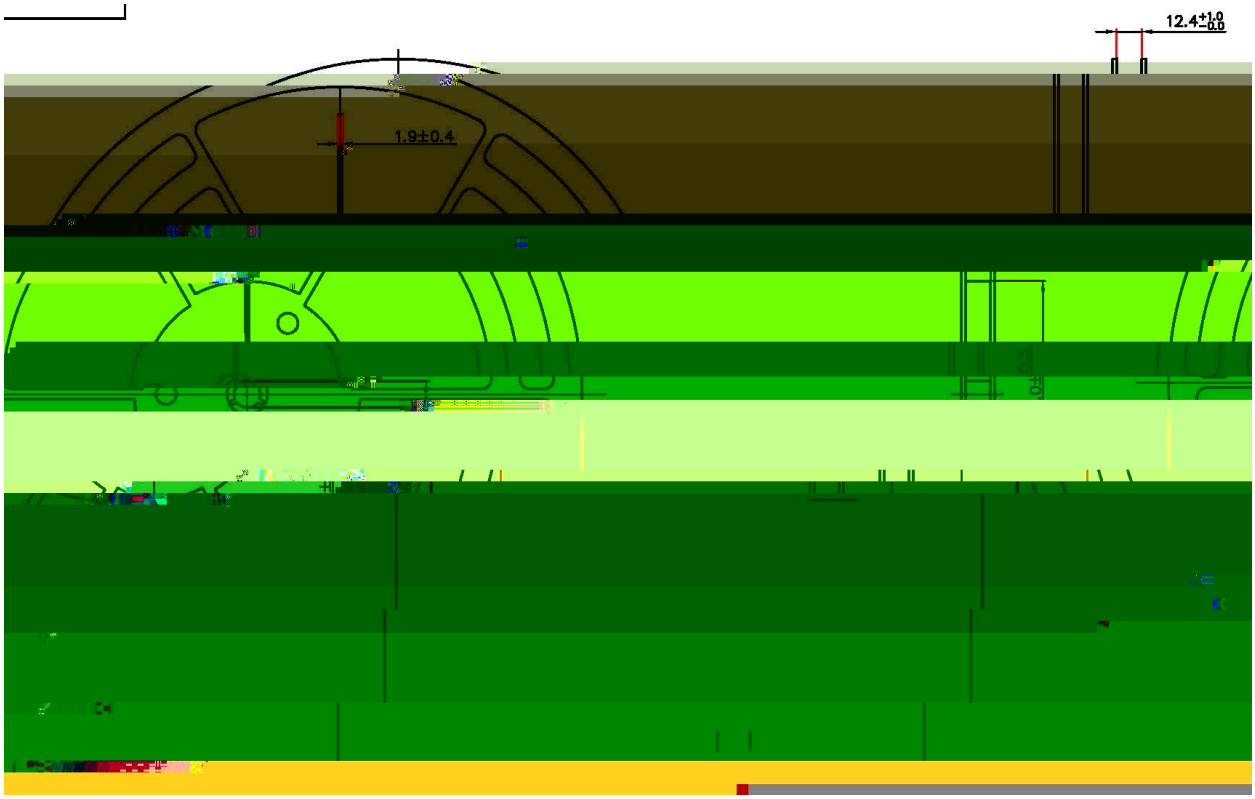


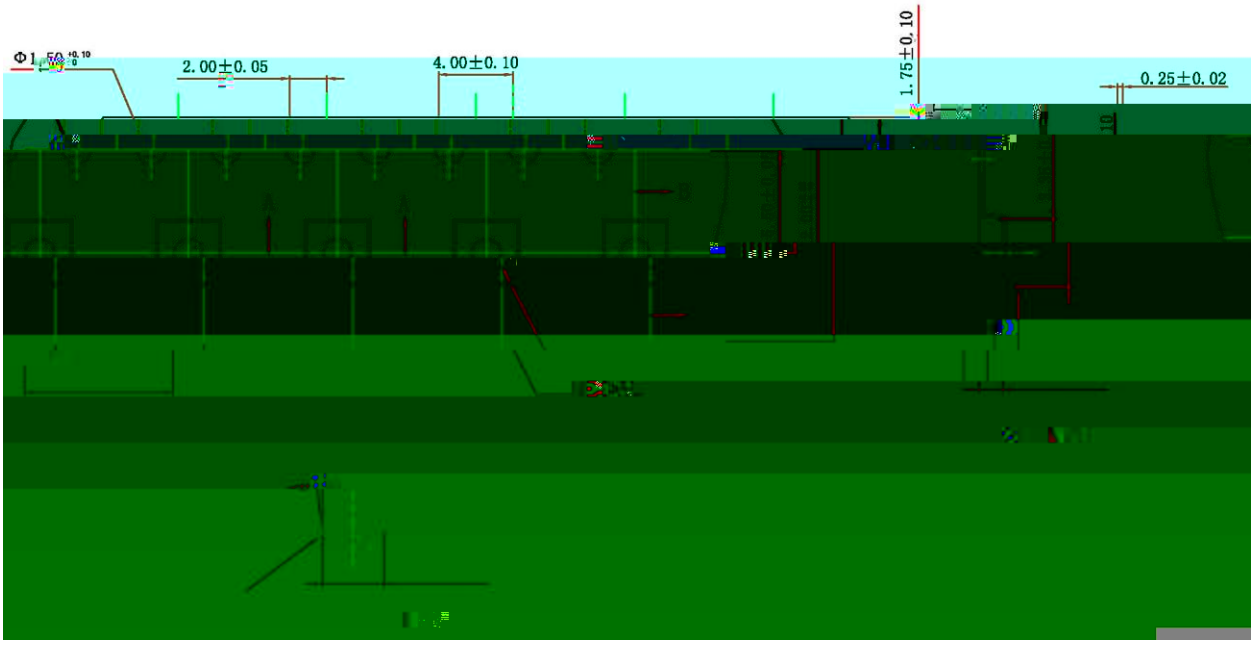


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| PN | DESCRIPTION | COMMENTS |
|---|---|---|
| **SCT63240** | 20W High-Integration, High-Efficiency PMIC for Wireless Power Transmitter<br><br>Integrate a 5V-1A Step-down DC/DC converter compared with SC63140. | • VIN Input Voltage Range: 4.2V-20V<br>• PVIN Input Voltage Range: 1V-17V<br>• Up to 20W Power Transfer<br>• Integrated High Efficiency Full-Bridge Power Stage<br>• Integrated High Efficiency 5V-1A Step-down DC/DC Converter<br>• Optimized for EMI<br>• Build in 3.3V-200mA LDO<br>• Provide 2.5V Voltage Reference<br>• Integrated Input Current sense with ±2% accuracy for FOD and modulation<br>• 3.3V and 5V PWM Signal compatible<br>• Input Under-Voltage Lockout<br>• Over current protection<br>• 3mm*4mm QFN-19L Package |

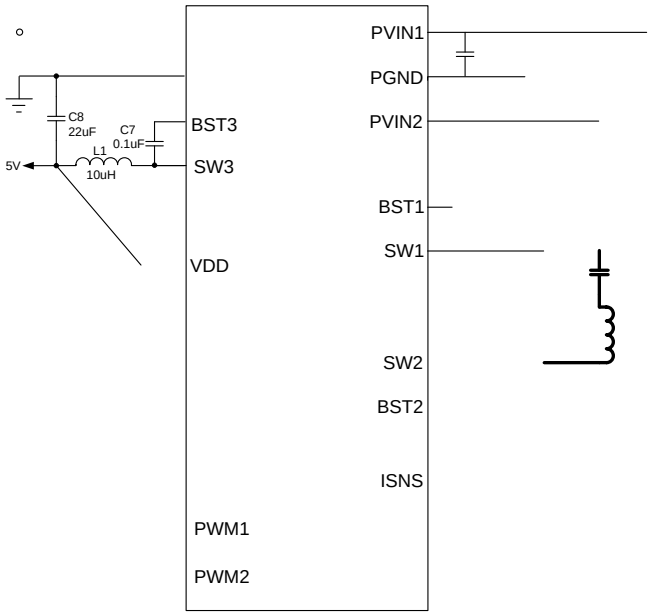


**Figure 19. SCT63240 Typical Application**

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**Silicon Content Technology Co., Ltd.**
#1 Floor 2 Building 15, Yard 33 Dijin Road, Haidian District, Beijing 100095
TEL (8610) 64779806 FAX: (8610) 64779806 www.silicontent.com© Silicon Content Technology