- Synchronous DCDC Buck Controller
  - 5.5V-100V Wide Input Range
  - 0.8V-60V Adjustable Output Voltage
  - 0.8V±1% Reference Voltage
  - 40ns Minimum t_{ON}
  - Selectable Diode Emulation or FPWM
- 7.5-V Gate Drivers
  - 2.3-A Source and 3.5-A Sink Current
  - *f* Low-side Soft Start for prebiased Start-
    Transient Response
  - Voltage-mode control with line feedforward
  - High Gain Bandwidth Error Amplifier
- Protection Features for Robustness
  - Adjustable Soft Start time
  - Hiccup-mode Overcurrent Protection

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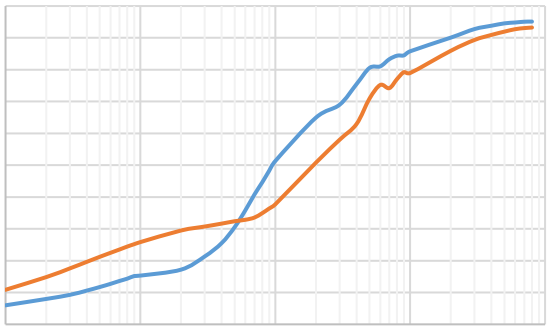
Parameter	Condition	Value
Input Voltage	DC up to 85V	15V-85V
Output Voltage	Iout=0A~8A	12V ± 1%
Output Current	Continuous DC current	8A



EV82A30-B-04A Evaluation Board Top View

SCT82A30 Efficiency, Freq.=400KHz

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/T1_10 1 Tf 0 0 0 rg 0 0 0 RG [(Evaluation)-47(board)-46(EV82A30-B-01A)-46(is)-47(easy)-46(to)-47(set)-46(up)-46(to)-47(evaluate)-46(the)-47(performance)-46(of)-47(SCT82A30)-46(synchronous)-47(step-)] TJ ET 0.000000912 0.612 792 reW* nBT/F1 9.96 Tf
down DCDC converter. Refer to Figure 1 for proper measurement equipment setup and follow the procedure below:

1. Place jumpers in the following positions:
   - VIN,GND : Connect the power supply to the input of converter.
   - VOUT,GND : Connect the load to the output of converter.
   - VIT(c)

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NOTE: When measuring the voltage ripple, care must be taken to avoid a long ground lead on the oscilloscope probe. Measure the input or output voltage ripple by touching the probe tip directly across relevant capacitor of VIN or VOUT. See Figure 2 for proper scope probe technique.

Figure 2. Measuring Voltage Ripple across Terminals or Directly Across Ceramic Capacitor

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Table 2. SCT82A30 EVM Bills of Materials

Manufacture	Part Number	Designator

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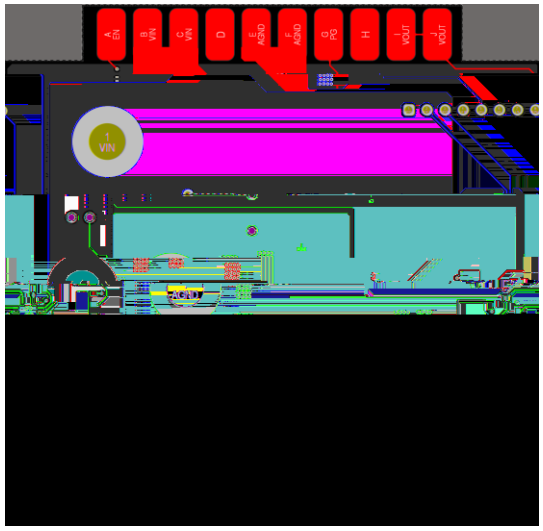

Figure 4. Top Layer

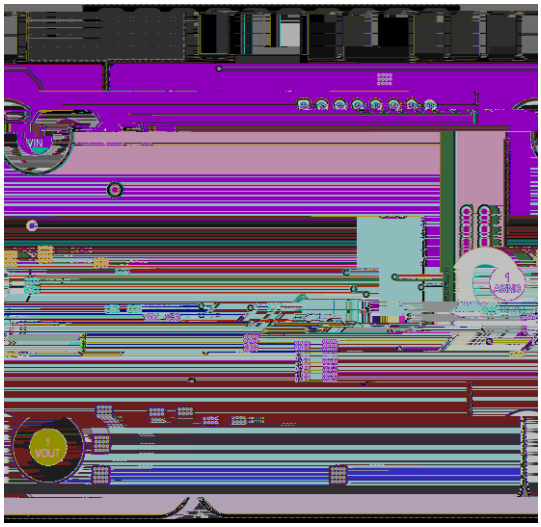

Figure 5. Internal 1 Layer

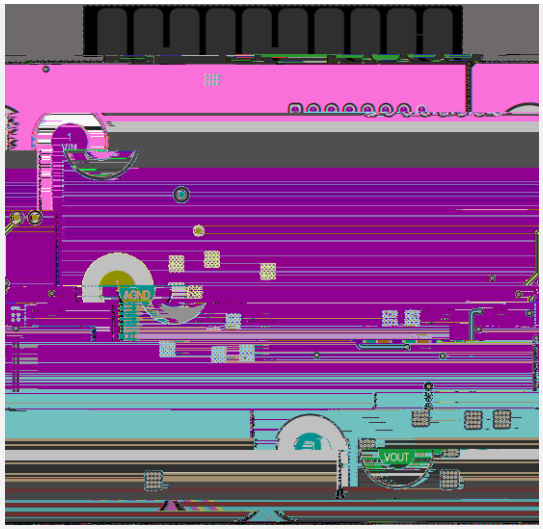

Figure 6. Internal 2 Layer

Figure 7. Bottom Layer

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Vin=48V, Vout=12V, unless otherwise noted

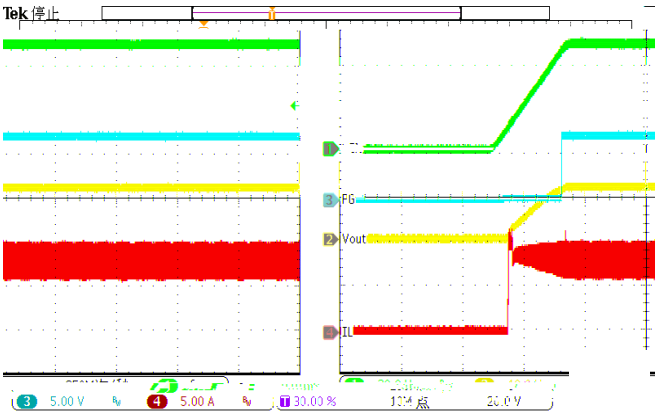

Figure 8. Power Up
(CH-1: Vin, CH-2: Vout, CH-3: PG, CH-IL)

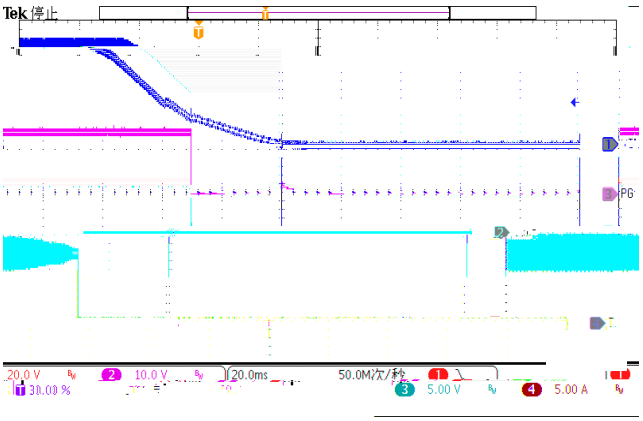

Figure 9. Power Down
(CH-1: Vin, CH-2: Vout, CH-3: PG, CH-IL)

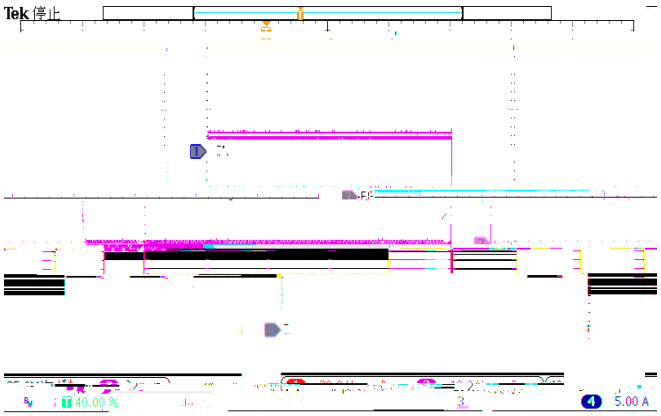

Figure 10. Startup at Output Hard-short
(CH-1: Vin, CH-2: Vout, CH-3: PG, CH-IL)

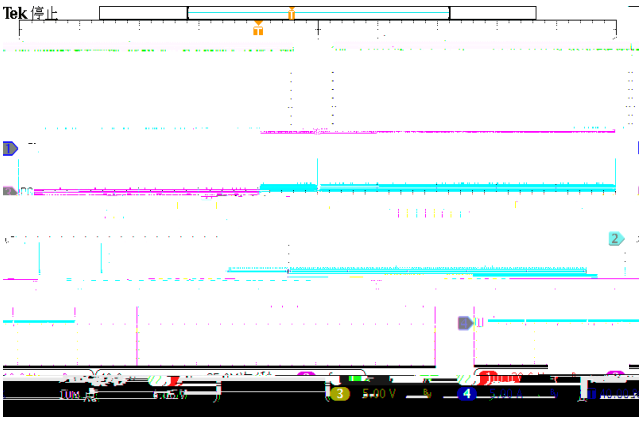

Figure 11. Output Hard-short and Recovery
(CH-1: Vin, CH-2: Vout, CH-3: PG, CH-IL)

Figure 12. Load Transient
(2A-6A, SR=1600mA/us, CH-4: Iout, CH-2: Vout)

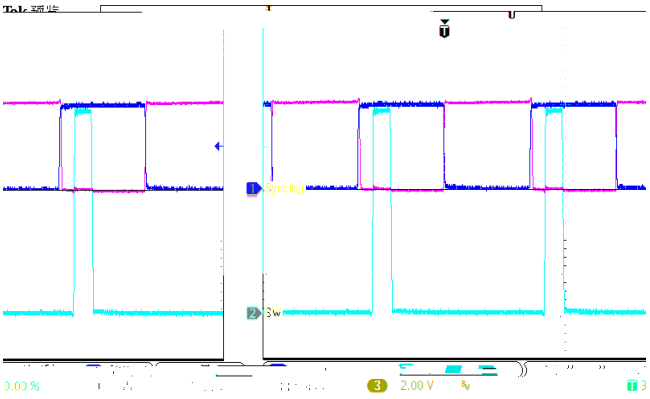

Figure 13. SYNCIN and SYNCOUT
(CH-1: SYCNIN, CH-2: SW, CH-3: SYNCOUT)

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Figure 14.
(CH-

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Overcurrent Protection

The EVM implements current sense schemes , using the on-state resistance of the low-side MOSFET, limiting the inductor current during an overload or output short-circuit condition. The controller senses the inductor current during the PWM off-time when LO is high.

If an application requires a higher current, R7 can be used to achieve an expected system current. The current limit threshold can be calculated by Equation 4.

$$_7 = \frac{-\Delta \quad /2}{200} \cdot \quad (\quad) \; 2 \tag{4}$$

Under Voltage Lockout Threshold

The SCT82A30 are enabled when the VIN pin voltage rises about 5.5V and the EN pin voltage exceeds the enable threshold of 1.2V.

If an application requires a higher system under voltage lockout threshold, two external resistors divider (R2 and R3) in Figure 16 can be used to achieve an expected system UVLO. The UVLO rising and falling threshold can be calculated by Equation 5 and Equation 6 respectively.

$$_2 = \frac{(\quad) - \quad (\quad)}{} \tag{5}$$

$$_3 = \; _2 \cdot \frac{}{(\quad) -} \tag{6}$$

where:

- $V_{IN(ON)}$ is the rising threshold of Vin UVLO.
- $V_{IN(OFF)}$ is the falling threshold of Vin UVLO

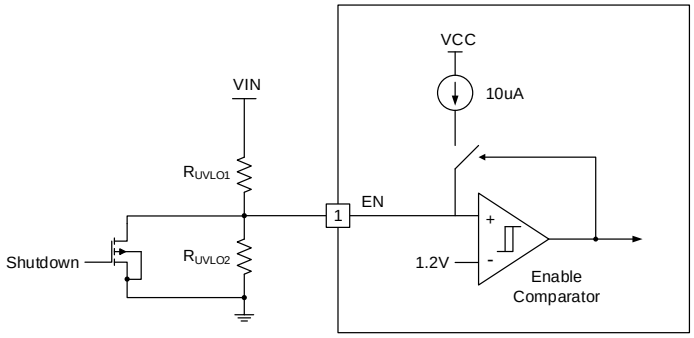

Figure 16. VIN UVLO Programmable by EN Dividers

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IMPORTANT NOTICE

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